Intra-Rack Resource Disaggregation Using Emerging Photonics

EMPOWERING OPEN.



Special Focus Optics

Intra-Rack Resource Disaggregation Using Emerging Photonics

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CHANGING WHAT'S POSSIBLE





BERKELEY LAB

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Resources in HPC are Underutilized

CDF memory occupied (%) node-wide statistics 100 Haswell KNL 80 75% 60 CDF (%) 40 20 0 17.4% 20 40 50.1% 60 80 100 0 Memory occupied (%)

G Michelogiannakis et al., "A Case for Intra-Rack Resource Disaggregation", ACM TACO 2022

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Resources in HPC are Underutilized



G Michelogiannakis et al., "A Case for Intra-Rack Resource Disaggregation", ACM TACO 2022



Intra-Rack Disaggregation Suffices

Probability for a CPU to cross rack boundary per resource



G Michelogiannakis et al., "A Case for Intra-Rack Resource Disaggregation", ACM TACO 2022



Towards Racks That Pool and Compose

Current server

Disaggregated rack

OWERING OPER



EMP



Photonic-Based Hardware Implementation





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sources



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Scaling Up To a Rack





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All-to-All Optical Switch

- Popular example: arrayed waveguide grating routers (AWGRs). All-to-all connectivity. Equal number of wavelengths from every source to every destination
- <u>State of the art example</u>: 400 x 400, 400 wavelengths per port, 25 GHz bandwidth per wavelength
- Y. Hida et al., "400-channel 25-ghz spacing arrayed-waveguide grating covering a full range of c- and lbands," in OFC 2001
- <u>Challenge</u>: Single wavelength's bandwidth may not be adequate. Requires indirect routing



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B Lin., "Generalization of an Optical ASA Switch", 2019



Spatial Optical Switch

- Popular examples: microelectromechanical systems (MEMS), microring resonators (MRRs)
- All wavelengths are connected from one port to another port
- <u>State of the art example</u> (MEMS): 240x240, one wavelength per port
- <u>Challenge</u>: Quantization of bandwidth. For example, 21 wavelengths escape an MCM



Q Cheng et al., "Photonic Switching in High Performance Datacenters", 2018



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Other Considerations

- "Intermediate" optical switches exist: Wave-selective
- Wave-selective and spatial switches reconfigure in micro to milli seconds
- CXL can be the link protocol
- Forward error correction can achieve necessary bit error rates with only an additional 5ns latency
- With modern photonic links, **we meet all design goals**. But what about the additional latency?



Speedup Over Electronic Switches

CPU timing CPU 000 GPU





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[Call to Action]

- Lets build efforts on the usability and programmability of resource-disaggregated systems: resource allocation algorithms, usage monitoring, programming models, runtime management, etc.
- Contact the speaker: mihelog@lbl.gov
- More information on the project ecosystem:
 - https://arpa-

e.energy.gov/sites/default/files/Columbia_Bergman_ENLITENED_Annual_Meetin g.pdf



Thank you!

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