Roofline Performance Modeling for HPC and Deep Learning Applications

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Schedule
9:00am  Introduction to Roofline  Samuel Williams
9:30am  NVProf Methodology/demo  Yunsong Wang
10:00am Rooftline Use Cases  Charlene Yang
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Introduction to the Roofline Model

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You just bought a $10,000 throughput-optimized GPU!

Are you making good use of your investment?
You could just run benchmarks

- Imagine running a mix of benchmarks or kernels…
- GFLOP/s alone may not be particularly insightful
- speedup relative to a Xeon may seem random

- We need a quantitative model that defines **Good Performance**
What is “Good” Performance?

- Good Performance is tied to “Efficient” execution
- Two fundamental requirements …

1. Must operate the GPU in the throughput-limited regime
   *not sensitive to Amdahl effects, D2H/H2D transfers, launch overheads, etc…*

2. Must attain high utilization of the GPU’s **compute** and/or **bandwidth** capabilities
Roofline Model

- **Roofline Model** is a throughput-oriented performance model
- applies to x86, ARM, POWER CPUs, GPUs, Google TPUs, FPGAs, etc…
- Helps quantify *Good Performance*

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1 Jouppi et al, "In-Datacenter Performance Analysis of a Tensor Processing Unit", ISCA, 2017.

https://crd.lbl.gov/departments/computer-science/PAR/research/roofline
Reduced Model

- GPU architectures can be complex
- Don’t model / simulate full architecture
- Make assumptions on performance and usage…
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  - Sufficient cache bandwidth/capacity
Reduced Model

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- Don’t model / simulate full architecture
- Make assumptions on performance and usage…
  - Peak GFLOP/s on data in L1
  - Load-balanced SPMD code
  - Sufficient cache bandwidth/capacity
  - Basis for DRAM Roofline Model
(DRAM) Roofline

- Any given loop nest will perform:
  - Computation (e.g. FLOPs)
  - Communication (e.g. moving data to/from DRAM)

- With perfect overlap of communication and computation...
  - Run time is determined by whichever is greater

\[
\text{Time} = \max \left\{ \frac{\#\text{FLOPs}}{\text{Peak GFLOP/s}}, \frac{\#\text{Bytes}}{\text{Peak GB/s}} \right\}
\]
Any given loop nest will perform:
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\[
\frac{\text{Time}}{\#\text{FLOPs}} = \max \left\{ \frac{1}{\text{Peak GFLOP/s}}, \frac{\#\text{Bytes}}{\#\text{FLOPs}} / \text{Peak GB/s} \right\}
\]
Any given loop nest will perform:
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\frac{\text{#FLOPs}}{\text{Time}} = \min \left\{ \text{Peak GFLOP/s}, \frac{\text{#FLOPs}}{\text{#Bytes}} \times \text{Peak GB/s} \right\}
\]
Any given loop nest will perform:
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With perfect overlap of communication and computation...
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\[
\text{GFLOP/s} = \min \left\{ \frac{\text{Peak GFLOP/s}}{\text{AI}}, \text{Peak GB/s} \right\}
\]

\text{AI (Arithmetic Intensity)} = \frac{\text{FLOPs}}{\text{Bytes (as presented to DRAM)}}
Arithmetic Intensity

- Measure of data locality (data reuse)
- Ratio of **Total Flops** performed to **Total Bytes** moved
- For the DRAM Roofline…
  - Total Bytes to/from DRAM
  - Includes all cache and prefetcher effects
  - Can be very different from total loads/stores (bytes requested)
  - Equal to ratio of sustained GFLOP/s to sustained GB/s (time cancels)
(DRAM) Roofline Model

\[
\text{GFLOP/s} = \min \left\{ \text{Peak GFLOP/s, AI} \times \text{Peak GB/s} \right\}
\]

- Plot Roofline bound using Arithmetic Intensity as the x-axis
- Log-log scale makes it easy to doodle, extrapolate performance along Moore’s Law, etc…

AI (Arithmetic Intensity) = FLOPs / Bytes (moved to/from DRAM)
(DRAM) Roofline Model

\[ \text{GFLOP/s} = \min \left\{ \frac{\text{Peak GFLOP/s}}{\text{AI}} \times \text{Peak GB/s} \right\} \]

- Plot Roofline bound using Arithmetic Intensity as the x-axis
- **Log-log scale** makes it easy to doodle, extrapolate performance along Moore’s Law, etc…

**Transition @ AI ==**

\[ \frac{\text{Peak GFLOP/s}}{\text{Peak GB/s}} = \text{‘Machine Balance’} \]
(DRAM) Roofline Model

\[
\text{GFLOP/s} = \min \left\{ \text{Peak GFLOP/s} \right\} \left( \frac{\text{AI}}{\text{Peak GB/s}} \right)
\]

AI (Arithmetic Intensity) = FLOPs / Bytes (moved to/from DRAM)

- Roofline tessellates this 2D view of performance into 5 regions…

- Transition @ AI == Peak GFLOP/s / Peak GB/s == ‘Machine Balance’
Roofline Example #1

- Typical machine balance is 5-10 FLOPs per byte…
  - 40-80 FLOPs per double to exploit compute capability
  - Artifact of technology and money
  - Unlikely to improve

- Consider STREAM Triad…

```c
#pragma omp parallel for
for(i=0;i<N;i++){  
z[i] = X[i] + alpha*Y[i];
}
```

- 2 FLOPs per iteration
- Transfer 24 bytes per iteration (read X[i], Y[i], write Z[i])
- $AI = 0.083$ FLOPs per byte == Memory bound
Conversely, 7-point constant coefficient stencil…

```c
#pragma omp parallel for
for(k=1;k<dim+1;k++){
  for(j=1;j<dim+1;j++){
    for(i=1;i<dim+1;i++){
      new[k][j][i] = -6.0*old[k][j][i] +
                      old[k][j][i-1] +
                      old[k][j][i+1] +
                      old[k][j-1][i] +
                      old[k][j+1][i] +
                      old[k-1][j][i] +
                      old[k+1][j][i];
    }
  }
}
```
Roofline Example #2

- Conversely, 7-point constant coefficient stencil...
  - 7 FLOPs
  - 8 memory references (7 reads, 1 store) per point
  - $AI = 7 / (8 \times 8) = 0.11$ FLOPs per byte
    (measured at the L1)

```c
#pragma omp parallel for
for(k=1;k<dim+1;k++){
  for(j=1;j<dim+1;j++){
    for(i=1;i<dim+1;i++){
      new[k][j][i] = -6.0*old[k][j][i] + old[k][j][i-1] + old[k][j][i+1] + old[k][j-1][i] + old[k][j+1][i] + old[k-1][j][i] + old[k+1][j][i];
    }
  }
}
```
Roofline Example #2

- Conversely, 7-point constant coefficient stencil...
  - 7 FLOPs
  - 8 memory references (7 reads, 1 store) per point
  - Ideally, cache will filter all but 1 read and 1 write per point

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#pragma omp parallel for
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    for(j=1;j<dim+1;j++){
        for(i=1;i<dim+1;i++){
            new[k][j][i] = -6.0*old[k][j][i] + old[k][j][i-1] + old[k][j][i+1] + old[k][j-1][i] + old[k][j+1][i] + old[k-1][j][i] + old[k+1][j][i] + old[k+1][j][i];
        }
    }
}
```
Conversely, 7-point constant coefficient stencil…

- 7 FLOPs
- 8 memory references (7 reads, 1 store) per point
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\[ \frac{7}{8+8} = 0.44 \text{ FLOPs per byte (DRAM)} \]

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== memory bound, but 5x the FLOP rate as TRIAD

```c
#pragma omp parallel
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        for(i=1;i<dim+1;i++)
            new[k][j][i] = -6.0*old[k][j][i] + old[k][j][i-1] + old[k][j][i+1] + old[k][j-1][i] + old[k][j+1][i] + old[k-1][j][i] + old[k+1][j][i];
```
What is “Good” Performance?

- Think back to our mix of loop nests (benchmarks)…

![Bar chart showing FLOP/s vs Kernel]
What is “Good” Performance?

- Think back to our mix of benchmarks (kernels)
- We can sort kernels by their arithmetic intensity…
What is “Good” Performance?

- Think back to our mix of benchmarks (kernels)
- We can sort kernels by their arithmetic intensity…
- … and compare performance relative to machine capabilities
What is “Good” Performance?

- Kernels near the roofline are making **good use** of computational resources
What is “Good” Performance?

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  - kernels can have low performance (GFLOP/s), but make good use (%STREAM) of a machine
What is “Good” Performance?

- Kernels near the roofline are making **good use** of computational resources
  - kernels can have low performance (GFLOP/s), but make good use (%STREAM) of a machine
  - kernels can have high performance (GFLOP/s), but still make poor use of a machine (%peak)
How can performance ever be below the Roofline?
How can performance be below the Roofline?

- Does one always attain either…
  - Peak DRAM Bandwidth
  - Peak FLOP/s

- Theoretical vs. Empirical
  - Use benchmarked GFLOP/s and GB/s
  - Application FLOPs can be underestimated (how many FLOPs is a divide?)

- Bottlenecks other than DRAM and FLOP/s…
  - Insufficient cache bandwidth + locality
  - Didn’t use FMA / Vectors / Tensors / …
  - Too many non-FP instructions
  - etc…
Below the Roofline?
Memory Hierarchy and Cache Bottlenecks
Memory Hierarchy

- GPUs have multiple levels of memory/cache
  - Registers
  - L1, L2, cache
  - HBM (GPU device memory)
  - DDR (host memory)
Memory Hierarchy

- GPUs have different bandwidths for each level
Memory Hierarchy

- GPUs have different bandwidths for each level
  - different machine balances for each level
Memory Hierarchy

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- Applications have locality in each level
  - different data movements for each level
Memory Hierarchy

- GPUs have different bandwidths for each level
  - different machine balances for each level

- Applications have locality in each level
  - different data movements for each level
  - different **arithmetic intensity** for each level
Cache Bottlenecks

For each additional level of the memory hierarchy, we can add another term to our model…

\[
\text{GFLOP/s} = \min \left\{ \text{Peak GFLOP/s}, \ A_{\text{DRAM}} \times \text{DRAM GB/s} \right\}
\]

\( A_{l_x} \) (Arithmetic Intensity at level “\( x \)”) = FLOPs / Bytes (moved to/from level “\( x \)”)

\[\text{GFLOP/s} = \min \left\{ \frac{\text{FLOPs}}{\text{Bytes moved to/from level } l_x}, \ A_{\text{DRAM}} \times \text{DRAM GB/s} \right\}\]
Cache Bottlenecks

- For each additional level of the memory hierarchy, we can add another term to our model...

\[
\text{GFLOP/s} = \min \left\{ \text{Peak GFLOP/s}, \ A_{\text{DRAM}} \times \text{DRAM GB/s}, \ A_{L2} \times \text{L2 GB/s} \right\}
\]

\(A_{x}\) (Arithmetic Intensity at level “x”): FLOPs / Bytes (moved to/from level “x”)
Cache Bottlenecks

- For each additional level of the memory hierarchy, we can add another term to our model…

\[
\text{GFLOP/s} = \min \left\{ \begin{array}{l}
\text{Peak GFLOP/s} \\
\text{Al}_{\text{DRAM}} \times \text{DRAM GB/s} \\
\text{Al}_{L2} \times L2 \text{ GB/s} \\
\text{Al}_{L1} \times L1 \text{ GB/s}
\end{array} \right. 
\]

\( \text{Al}_x \) (Arithmetic Intensity at level “x”) = FLOPs / Bytes (moved to/from level “x”)
Cache Bottlenecks

- Plot equation in a single figure…
  - “Hierarchical Roofline” Model
Cache Bottlenecks

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  - Bandwidth ceiling (diagonal line) for each level of memory
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  - performance is ultimately the minimum of these bounds
Cache Bottlenecks

- Plot equation in a single figure...
  - “Hierarchical Roofline” Model
  - Bandwidth ceiling (diagonal line) for each level of memory
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  - Performance is ultimately the minimum of these bounds

- If L2 bound, we see HBM dot well below HBM ceiling
Cache Bottlenecks

- Widely separated Arithmetic Intensities indicate high reuse in the cache
Cache Bottlenecks

- Widely separated Arithmetic Intensities indicate high reuse in the cache
- Similar Arithmetic Intensities indicate effectively no cache reuse (== streaming)
Below the Roofline?

FMA, Reduced Precision, Tensor Cores
Return of CISC

- Vectors have their limits (finite DLP, register file energy scales with VL, etc…)
- Death of Moore’s Law is reinvigorating Complex Instruction Set Computing (CISC)

- Modern CPUs and GPUs are increasingly reliant on special (fused) instructions that perform multiple operations (fuse common instruction sequences)...
  - FMA (Fused Multiply Add): \( z = a \cdot x + y \) …\( z, x, y \) are vectors or scalars
  - 4FMA (Quad FMA): \( z = A \cdot x + z \) …\( A \) is a FP32 matrix; \( x, z \) are vectors
  - WMMA (Tensor Core): \( Z = A \cdot B + C \) …\( A, B \) are FP16 matrices; \( Z, C \) are FP32

- If instructions are a mix or scalar (predicated), vector, and matrix operations, performance is now a weighted average of them.
Return of CISC

- Consider NVIDIA Volta GPU...
  - ~100 TFLOPs for FP16 Tensor
  - 15 TFLOPS for FP32 FMA
  - 7.5 TFLOPs for FP32 Add

- DL applications mix Tensor, FP16, and FP32

- DL performance may be well below nominal Tensor Core peak
Return of CISC

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- DL applications mix Tensor, FP16, and FP32
- DL performance may be well below nominal Tensor Core peak
- The actual mix of instructions introduces an effective ceiling on performance…

Diagram: Attainable FLOP/s vs. Arithmetic Intensity (FLOP:Byte)
Think about classifying apps by instruction mix...

- Heavy floating-point (traditional FLOP Roofline)
- Mix of integer and floating-point (FPU starvation)
- Integer-only (e.g. bioinformatics, graphs, etc…)
- Mixed precision (e.g. deep learning)
NVIDIA GPU Instruction Roofline

- Instructions per second? Instructions per Byte?

- What is an ‘Instruction’ on a GPU?
  - Thread-level hides issue limits?
  - Warp-level hides predication effects?
  - Scale non-predicated threads down by the warp size (divide by 32)

- Naively, one would think instruction intensity should use ‘bytes’

- GPUs access memory using ‘transactions’
  - 32B for global/local/L2/HBM
  - 128B for shared memory
  - “Instructions/Transaction” preserves traditional Roofline, but enables a new way of understanding memory access
Instruction Roofline

$$\text{GFLOP}/s = \min \left\{ \text{Peak GFLOP}/s, \quad \text{AI}_{\text{DRAM}} \times \text{DRAM GB}/s \right\}$$
Instruction Roofline

\[ \text{GFLOP/s} = \min \left\{ \frac{\text{Peak GFLOP/s}}{A_{\text{DRAM}} \times \text{DRAM GB/s}} \right\} \]

\[ \text{GIPS} = \min \left\{ \frac{\text{Peak GIPS}}{I_{\text{DRAM}} \times \text{DRAM GB/s}} \right\} \]

Instructions per Byte

Nan Ding, Samuel Williams, "An Instruction Roofline Model for GPUs", PMBS, November, 2019.
Instruction Roofline on GPUs

\[ \text{GFLOP/s} = \min \left\{ \frac{\text{Peak GFLOP/s}}{\text{AI}_{\text{DRAM}} \times \text{DRAM GB/s}} \right\} \]

\[ \text{GIPS} = \min \left\{ \frac{\text{Peak GIPS}}{\text{II}_{\text{DRAM}} \times \text{DRAM GB/s}} \right\} \]

As the natural quanta for GPU memory access is a “transaction”...

Nan Ding, Samuel Williams, "An Instruction Roofline Model for GPUs", PMBS, November, 2019.
Instruction Roofline on GPUs

\[
\text{GFLOP/s} = \min \left\{ \text{Peak GFLOP/s} \right. \\
\left. \frac{A_I}{\text{DRAM}} \times \text{DRAM GB/s} \right\}
\]

\[
\text{GIPS} = \min \left\{ \text{Peak GIPS} \right. \\
\left. \frac{I_{II}}{\text{DRAM}} \times \text{DRAM GB/s} \right\}
\]

\[
\text{GIPS} = \min \left\{ \text{Peak GIPS} \right. \\
\left. \frac{I_{II}}{\text{DRAM}} \times \text{DRAM GTXN/s} \right\}
\]

\[
I_{II} (\text{Instruction Intensity at level “x”}) = \frac{\text{Instructions}}{\text{Transactions (to/from level “x”)}},
\]

Nan Ding, Samuel Williams, "An Instruction Roofline Model for GPUs", PMBS, November, 2019.
Efficiency of Global Memory Access

- (Global)LDST Instruction Intensity has a special meaning / use…
  - Global LDST instructions / Global transactions
  - Numerator lower than nominal
  - Denominator can be lower than nominal L1 (no local or shared transactions)

- Denotes efficiency of memory access

- 3 “Walls” of interest:
  - ≥1 transaction per LDST instruction (all threads access same location)
  - ≤32 transactions per LDST instruction (gather/scatter or stride>=128B)
  - Unit Stride: 1 LDST per 8 transactions (double precision)
Efficiency of Shared Memory Access

- (Shared)LDST Instruction Intensity also has a special meaning / use
  - Shared LDST instructions / Shared transactions
  - II is similarly loosely related to nominal II

- Can be used to infer the number of bank conflicts

- 2 “Walls” of interest:
  - Minimum of 1 transaction per shared LDST instruction (*no bank conflicts*)
  - Maximum of 32 transactions per shared LDST instruction (*all threads access different lines in the same bank*)

Nan Ding, Samuel Williams, "An Instruction Roofline Model for GPUs", PMBS, November, 2019.
Instruction Roofline for Matrix Transpose

**Instruction Hierarchy & Thread Predication**
- **Naive**
  - High Stride Access
  - Bank conflicts are eliminated

**Global Memory Efficiency**
- **Theoretical Peak**: 489.6 warp GIPS
- **Global Memory Efficiency** not used

**Shared Memory Efficiency**
- **Theoretical Peak**: 489.6 warp GIPS
- **Shared Memory Efficiency**
  - Bank conflict on every access
  - Bank conflicts are eliminated

**Array Padding**
- **Improved L1 locality due to elimination of bank conflicts**

**Transpose in Shared Array**
- **Loss in L1 locality due to use of shared memory**

Nan Ding, Samuel Williams, "An Instruction Roofline Model for GPUs", PMBS, November, 2019.
Roofline Recap

Bounds performance
- Horizontal Lines = Compute Ceilings
- Diagonal Lines = Bandwidth Ceilings
- Bandwidth ceilings are parallel on log-log scale

- Collectively, ceilings define an upper limit on performance

Arithmetic Intensity
- Different intensity for each level of memory
- Total FLOPs / Total Data Movement
- Includes all cache effects

- Measure of a loop’s temporal locality

Plotting loops...
- Each loop has one dot per level of memory
- x-coordinate = AI at that level
- y-coordinate = GFLOP/s

- Proximity to associated ceiling is indicative of a performance bound

- Position of dots relative to each other is indicative of cache locality
Instruction Roofline Takeaway

**Traditional Roofline**
- Tells us about **performance** *(floating-point)*
- Intensity based on data locality (FLOPs / Bytes)
- Use of FMA, SIMD, vectors, tensors has no affect on intensity
- Presence of integer instructions has no affect on intensity.
- Reducing precision (64b, 32b, 16b) increases arithmetic intensity

**Instruction Roofline**
- Tells us about **bottlenecks** *(issue and memory)*
- Intensity based on **total** instructions and transactions
- Use of FMA, SIMD, vectors, tensors decreases intensity.
- Presence of integer instructions increases intensity.
- Reducing precision has no affect on intensity

**Memory Walls**
- Tells us about **efficiency** *(memory access)*
- Intensity based on LDST instructions and transactions
- Reducing precision shifts intensity and the unit-stride wall
What is Roofline used for?

- Understand performance differences between Architectures, Programming Models, implementations, etc…
  - Why do some Architectures/Implementations move more data than others?
  - Why do some compilers outperform others?

- Predict performance on future machines / architectures
  - Set realistic performance expectations
  - Drive for HW/SW Co-Design

- Identify performance bottlenecks & motivate software optimizations

- Determine when we’re done optimizing code
  - Assess performance relative to machine capabilities
  - Track progress towards optimality
  - Motivate need for algorithmic changes
Questions?