Introduction to the Roofine Model

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You just spent 6 months porting your application to GPUs

Are you done?







- Imagine profiling the mix of loop nests in an application when running on the GPU
 - GFLOP/s alone may not be particularly insightful
 - speedup relative to a Xeon may seem random





- Two fundamental aspects to "Good" performance...
- 1. Operating in the throughput-limited regime not sensitive to Amdahl effects, D2H/H2D transfers, launch overheads, etc...
- 2. making good use of the GPU's **compute** and/or **bandwidth** capabilities

> Ultimately, we need a quantitative model rather than qualitative statements like "good"



Roofline Model

- Roofline Model is a throughputoriented performance model
- Tracks rates not times
- Independent of ISA and architecture
- applies to CPUs, GPUs, Google TPUs¹, FPGAs, etc...
- Helps quantify Good Performance

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PERFORMANCE AND ALGORITHMS BeBOP BBOP EDGAR HIDGISAXS HDGMG ScIDAC SCIDAC TOP500 Previous Projects	Roofline Pee Roofline is a visually intuitive performan multicore, manycore, or accelerator prora performance figure. One can examine th limitations: Actine Contension Contensio Contension Contensio Contensio Contension	erformance resorarchitectures. Rather than si ce by combining locality, bandwidth te resultant Roofline figure in order model is Arithmetic Intensity. Arithh vector-vector increment (x[1]=y[1]) t of the vector size. Conversely, il locate cache architecture, the tr . 0.1041ogN and would grow slow ups 2 flops per byte. Finally, BLA:
Facebook 8 Google+ Coogle+ Twitter	0.1-1.0 flops per SomV BLAS1,2 Stencils (PDEs) Lattice I	r byte Typically < 2 flor thmetic FFTs, Spectral Methods
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https://crd.lbl.gov/departments/computer-science/PAR/research/roofline

Roofline Model





Reduced Model

- Superscalar architectures can be complex
- Don't model / simulate full architecture
- Created simplified processor architecture





Reduced Model

- Superscalar architectures can be complex
- Don't model / simulate full architecture
- Created simplified processor architecture
- Make assumptions on performance and usage...
 - o Cores can attain peak GFLOP/s on local data
 - Cores execute load-balanced SPMD code
 - NoC bisection bandwidth is sufficient
 - There is sufficient cache bandwidth and capacity such that they do not affect performance
 - Basis for DRAM Roofline Model





- Which takes longer?
 - o Data Movement
 - Compute?



Time = max { #FP ops / Peak GFLOP/s #Bytes / Peak GB/s



- Which takes longer?
 - o Data Movement
 - Compute?
- Is performance limited by compute or data movement?



Time
#FP ops= max1 / Peak GFLOP/s
#Bytes / #FP ops / Peak GB/s



- Which takes longer?
 - o Data Movement
 - Compute?
- Is performance limited by compute or data movement?



#FP ops
Time= min {Peak GFLOP/s
(#FP ops / #Bytes) * Peak GB/s



- Which takes longer?
 - o Data Movement
 - Compute?
- Is performance limited by compute or data movement?



GFLOP/s = min { AI * Peak GB/s

AI (Arithmetic Intensity) = FLOPs / Bytes (as presented to DRAM)



Arithmetic Intensity

- Measure of data locality (data reuse)
- Ratio of <u>Total Flops</u> performed to <u>Total Bytes</u> moved
- For the DRAM Roofline...
 - Total Bytes to/from DRAM
 - \circ $\,$ Includes all cache and prefetcher effects $\,$
 - Can be very different from total loads/stores (bytes requested)
 - Equal to ratio of sustained GFLOP/s to sustained GB/s (time cancels)



(DRAM) Roofline Model

GFLOP/s = min { AI * Peak GB/s

AI (Arithmetic Intensity) = FLOPs / Bytes (moved to/from DRAM)

- Plot Roofline bound using Arithmetic Intensity as the x-axis
- Log-log scale makes it easy to doodle, extrapolate performance along Moore's Law, etc...





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'Machine Balance'



(DRAM) Roofline Model

Peak GFLOP/s AI * Peak GB/s GFLOP/s = min

AI (Arithmetic Intensity) = FLOPs / Bytes (moved to/from DRAM)

Roofline tessellates this 2D view of performance into 5 regions...



Transition @ AI == Peak GFLOP/s / Peak GB/s == 'Machine Balance'



- Typical machine balance is 5-10
 FLOPs per byte...
 - o 40-80 FLOPs per double to exploit compute capability
 - Artifact of technology and money
 - o Unlikely to improve

Consider STREAM Triad...

#pragma omp parallel for for(i=0;i<N;i++){ Z[i] = X[i] + alpha*Y[i]; }

- 2 FLOPs per iteration
- Transfer 24 bytes per iteration (read X[i], Y[i], write Z[i])
- AI = 0.083 FLOPs per byte == Memory bound





Conversely, 7-point constant coefficient stencil...



<pre>#pragma omp parallel for</pre>
for(k=1;K <d1m+1;k++){< td=""></d1m+1;k++){<>
<pre>for(j=1;j<dim+1;j++){< pre=""></dim+1;j++){<></pre>
<pre>for(i=1;i<dim+1;i++){< pre=""></dim+1;i++){<></pre>
new[k][j][i] = -6.0*old[k][j][i]
+ old[k][j][i-1]
+ old[k][j][i+1]
+ old[k][j-1][i]
+ old[k][j+1][i]
+ old[k-1][j][i]
+ old[k+1][j][i];
}}}



- Conversely, 7-point constant coefficient stencil...
 - o 7 FLOPs
 - o 8 memory references (7 reads, 1 store) per point
 - AI = 7 / (8*8) = 0.11 FLOPs per byte (measured at the L1)

#pragma omp parallel for for(k=1;k<dim+1;k++){ for(j=1;j<dim+1;j++){ r(i=1,i<unit;i++){ new[k][j][i] = -6. *old[k][j][i] + old[k][j][i-1] + old[k][j][i+1] + old[k][j-1][i] + old[k][j+1][i] + old[k-1][j][i] + old[k-1][j][i] + old[k+1][j][i]





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 - 7 / (8+8) = 0.44 FLOPs per byte (DRAM)

```
#pragma omp parallel for
for(k=1;k<dim+1;k++){</pre>
for(j=1;j<dim+1;j++){</pre>
for(i=1;i<dim+1;i++){</pre>
 new[k][j][i] = -6.0*old[k ][j
                      <u>+ old[k ][j ][i-1]</u>
                      + old[k
                               ][i ][i+1]
                      + old[k
                               _][i-1][i
                      + old[k ][i+1][i
                      + old[k-1][i
                                      1ſi
                      + old[k+1][j _][i
                                           1:
}}}
```

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- Conversely, 7-point constant coefficient stencil...
 - 7 FLOPs Ο
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== memory bound, but 5x the FLOP rate as TRIAD

<pre>#pragma omp parallel for</pre>
<pre>for(k=1;k<dim+1;k++){< pre=""></dim+1;k++){<></pre>
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+ old[k][j][i-1]
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+ old[k][j+1][i]
+ old[k-1][j][i]
+ old[k+1][j][i];
}}}



Peak GFLOP/s GFLOP/s ≤ AI * HBM GB/s

7-point Stencil



 Think back to our mix of loop nests...





 We can sort kernels by arithmetic intensity...





- We can sort kernels by arithmetic intensity...
- ... and compare performance relative to machine capabilities





Kernels near the roofline are making good use of computational resources



50% of Peak



- Kernels near the roofline are making good use of computational resources
 - kernels can have <u>low performance</u> (GFLOP/s), but make good use (%STREAM) of a machine



50% of Peak



- Kernels near the roofline are making good use of computational resources
 - kernels can have low performance (GFLOP/s), but make good use (%STREAM) of a machine
 - kernels can have high performance (GFLOP/s), but still make poor use of a machine (%peak)





Roofline is made of two components

Machine Model

- Lines defined by peak GB/s and GF/s Ο (**Benchmarking**)
- Unique to each architecture Ο
- Common to all apps on that architecture Ο





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Machine Model

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Application Characteristics

- Dots defined by application GFLOP's and Ο GB's (Application Instrumentation)
- Unique to each application Ο
- Unique to each architecture Ο





General Performance Optimization Strategy

Get to the Roofline





General Performance Optimization Strategy

- Get to the Roofline
- Increase Arithmetic Intensity when bandwidth-limited
 - Reducing data movement increases AI





How can performance ever be below the Roofline?







Performance Below the Roofline?

Hierarchical Roofline Model

Charlene Yang, Thorsten Kurth, Samuel Williams, "Hierarchical Roofline analysis for GPUs: Accelerating performance optimization for the NERSC-9 Perlmutter system", Concurrency and Computation: Practice and Experience (CCPE), August 2019.



Arithmetic Intensity (FLOP:Byte)





Roofline Scaling Trajectories

Khaled Ibrahim, Samuel Williams, Leonid Oliker, "Performance Analysis of GPU Programming Models using the Roofline Trajectories". Scaling International **Symposium** Benchmarking, on Measuring and Optimizing (Bench), **BEST PAPER AWARD.** November 2019.

Instruction **Roofline Model**

Nan Ding, Samuel Williams, "An Instruction Roofline Model for GPUs", Performance Modeling, Benchmarking, and Simulation (PMBS), BEST PAPER AWARD, November 2019.



Additional FP Ceilings

Charlene Yang, Thorsten Kurth, Williams, Samuel "Hierarchical for GPUs: Roofline analysis Accelerating performance optimization for the NERSC-9 Perlmutter system", Concurrency and Computation: Practice and Experience (CCPE), August 2019.



Instruction Intensity (Warp Instructions per Transaction)



Summary



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Why We Use Roofline...

1. Determine when we're done optimizing code

- Assess performance relative to machine capabilities Ο
- Track progress towards optimality Ο
- Motivate need for algorithmic changes Ο
- 2. Identify performance bottlenecks & motivate software optimizations
- 3. Understand performance differences between Architectures, Programming Models, implementations, etc...
 - Why do some Architectures/Implementations move more data than others? Ο
 - Why do some compilers outperform others? Ο

4. Predict performance on future machines / architectures

- Set realistic performance expectations 0
- Drive for Architecture-Computer Science-Applied Math Co-Design Ο



Take away

- Roofline helps understand application performance relative to machine capabilities
 - just the beginning of the optimization process
 - Other bottleneck- or architecture-specific tools can be used to refine the process
- Roofline helps frame the conversation between...
 - **Application Developers**
 - **Computer Scientists**
 - **Applied Mathematicians**
 - **Processor Vendors**

...providing a common mental model and optimization language





Questions



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